연구실 소개

연세대학교 전기전자공학부

임베디드 시스템 및 컴퓨터 구조 연구실

노원우 교수

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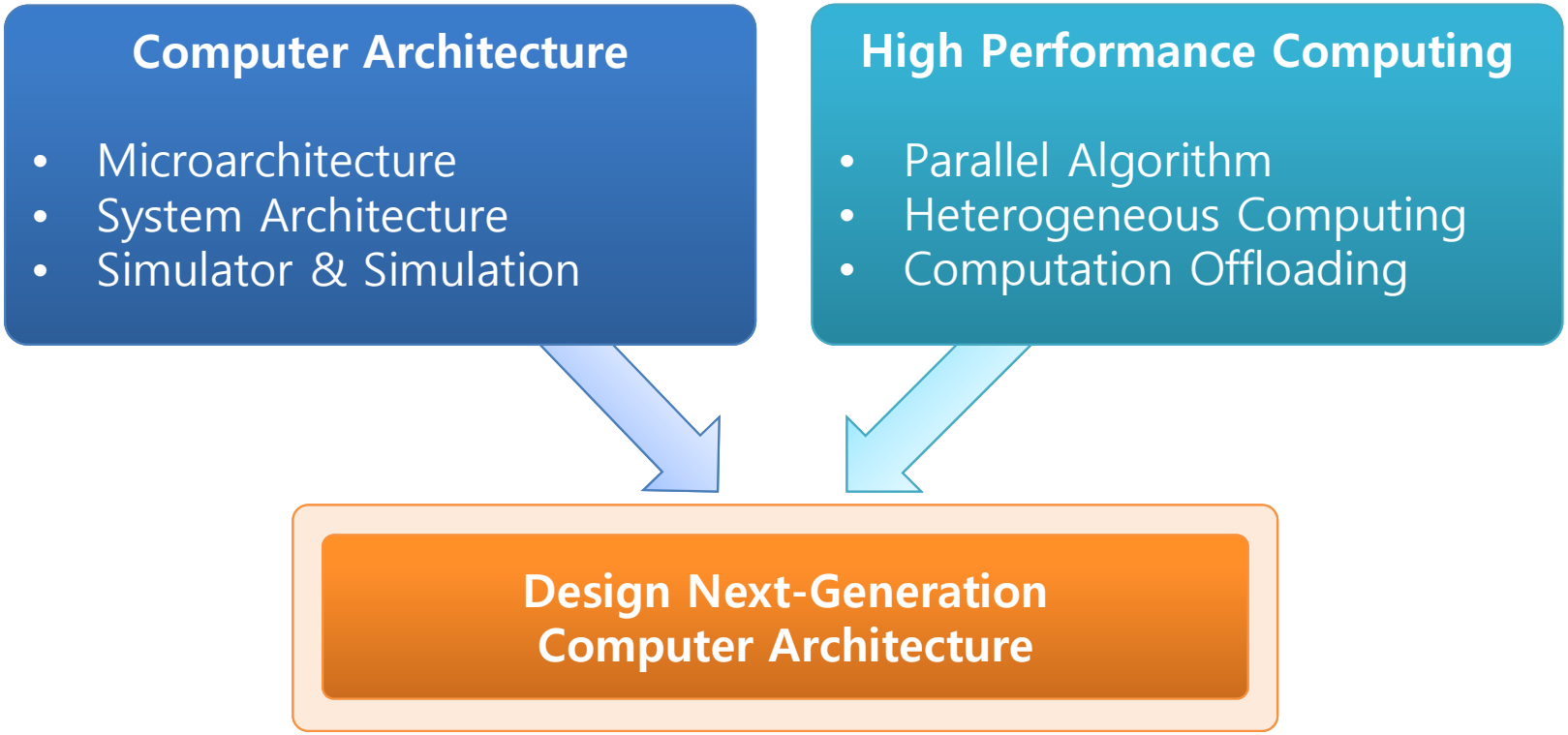
LAB. INTRODUCTION

- **Embedded Systems and Computer Architecture Lab.**



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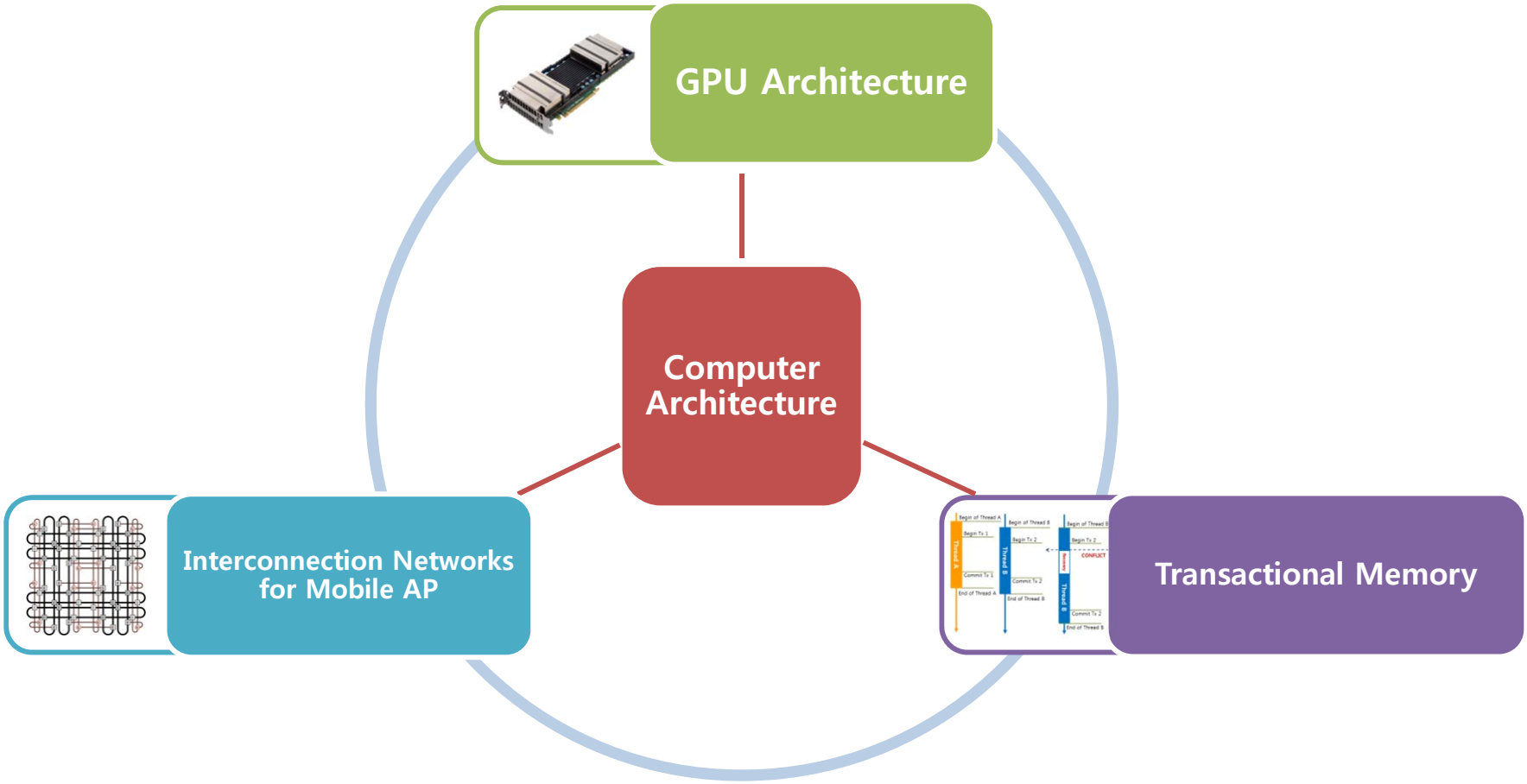
주 연구분야



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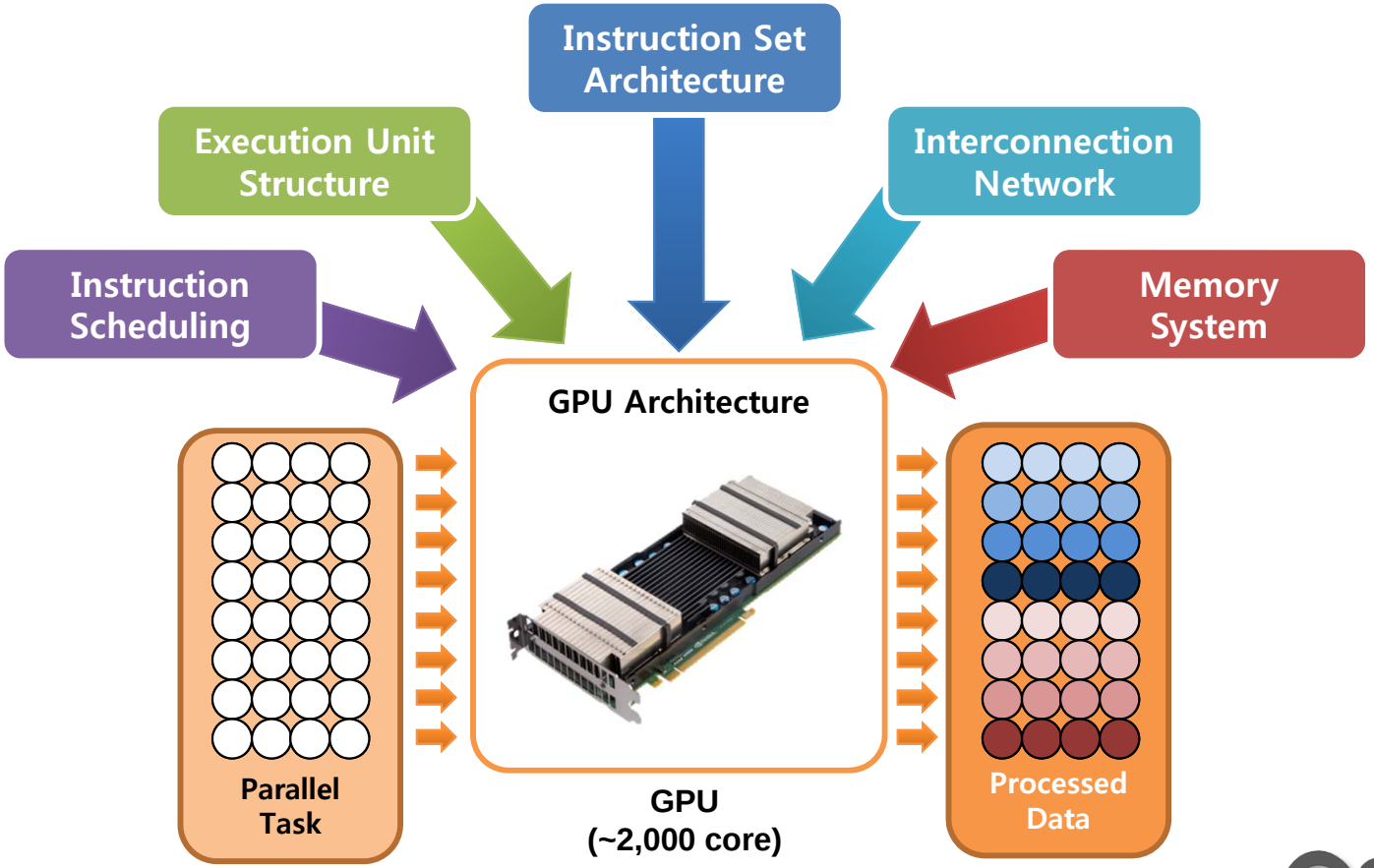
GPU Architecture Research

- **병렬 컴퓨팅을 위한 GPU Architecture 연구**
  - ✓ 대규모 연산에 적합한 GPU의 특성 분석 및 고효율/고성능 연산을 위한 GPU architecture 개선
  - ✓ GPU hardware resource의 최적 활용을 위한 software 지원



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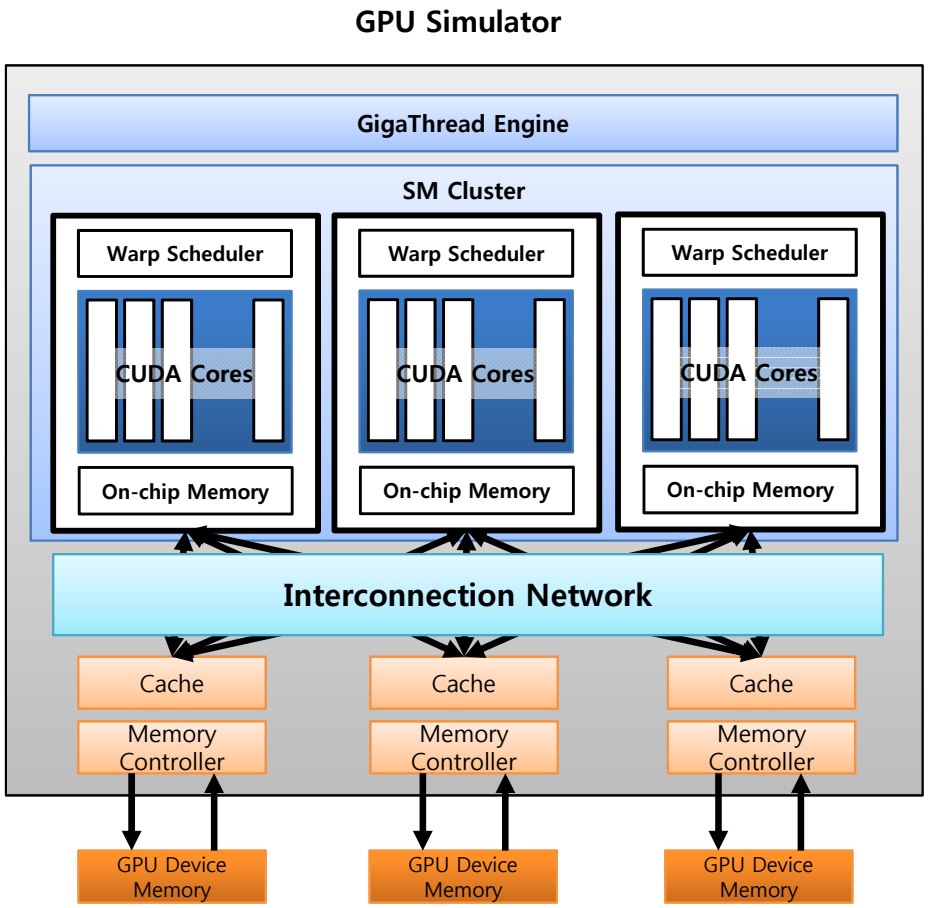
RESEARCH TOPIC(1) – SIMULATION

- **GPU Architecture Simulator**
  - ✓ Processor model, network, memory system 등 GPU의 주요 구성요소 simulation
  - ✓ Architecture 설계, 변경, 검증을 위한 연구 기반 제공



Processor Model
- Task Control Engine
- Thread Scheduling
- Instruction Group Scheduling
- Execution Unit
- On-chip Memory

Network
- Interconnection Network

Memory System
- Cache Memory
- Memory Controller
- DRAM

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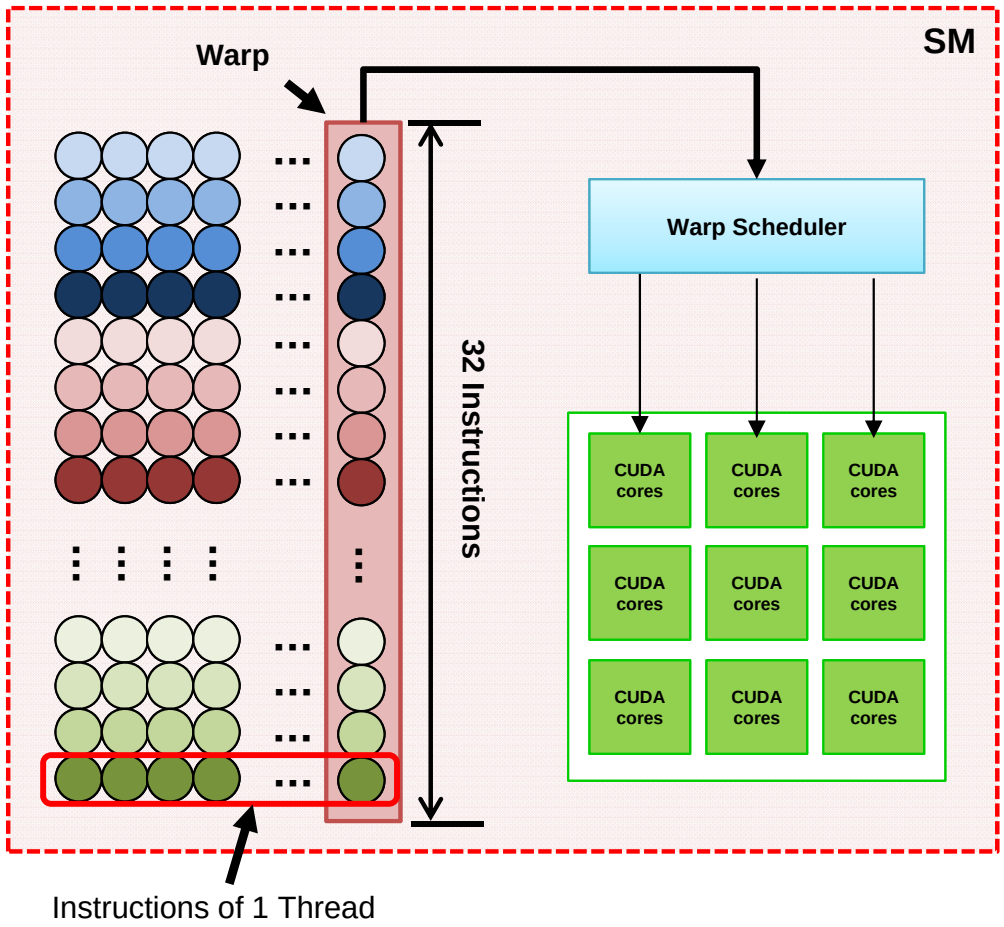
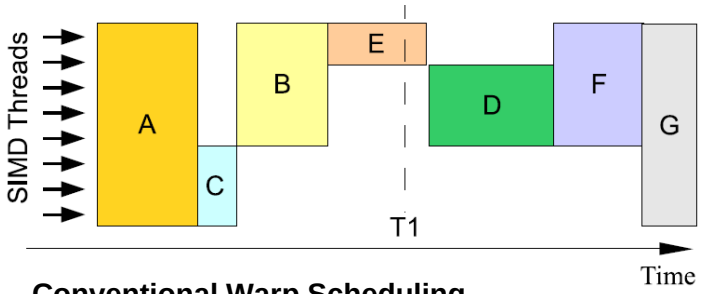
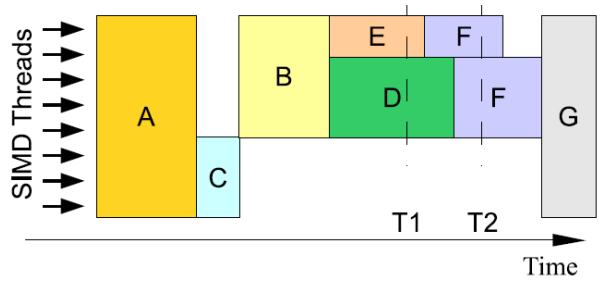
RESEARCH TOPIC(2) – ARCHITECTURE DESIGN

- **GPU Frontend Design Improvement**
  - ✓ GPU instruction의 set(warp) 구성 방법, 실행 순서, 방식 등 instruction scheduling 효율화를 통한 성능 향상 기법 연구
  - ✓ Simulator를 활용한 scheduler 구조 변경 및 검증





Conventional Warp Scheduling



Dynamic Warp Subdivision*

*Ref: Meng et al., *Dynamic Warp Subdivision for Integrated Branch and Memory Divergence Tolerance* (ISCA'10)

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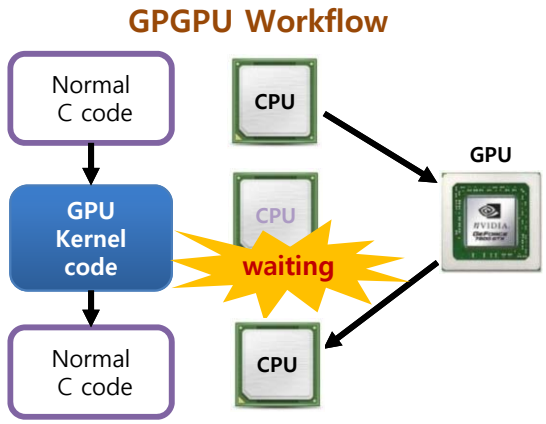
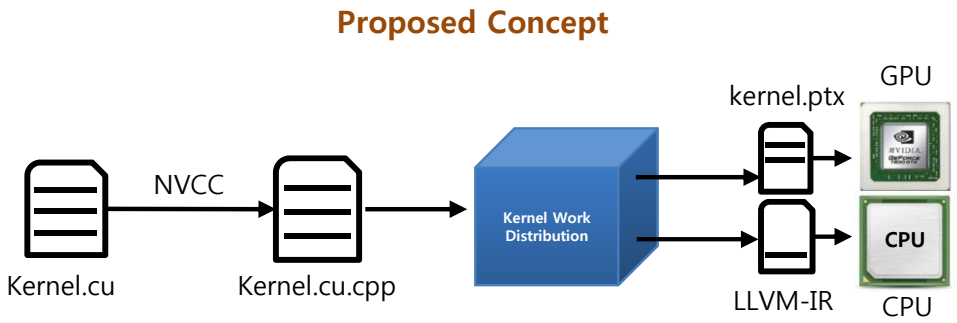
RESEARCH TOPIC(3) – OPTIMIZATION

- **GPGPU Application 최적화**
  - ✓ GPU architecture에 적합한 parallel algorithm 및 hardware utilization 최적화 연구
- **협력 연산을 통한 GPGPU Application 성능 개선 연구**
  - ✓ GPGPU application의 CPU 자원 미활용 문제
  - ✓ CPU의 유휴 자원을 GPGPU application 처리에 이용
  - ✓ GPGPU code translation : kernel work partitioning + LLVM compilation technique
  - ✓ GPU 및 x86 CPU의 협력 연산 수행을 통한 application 처리성능 향상





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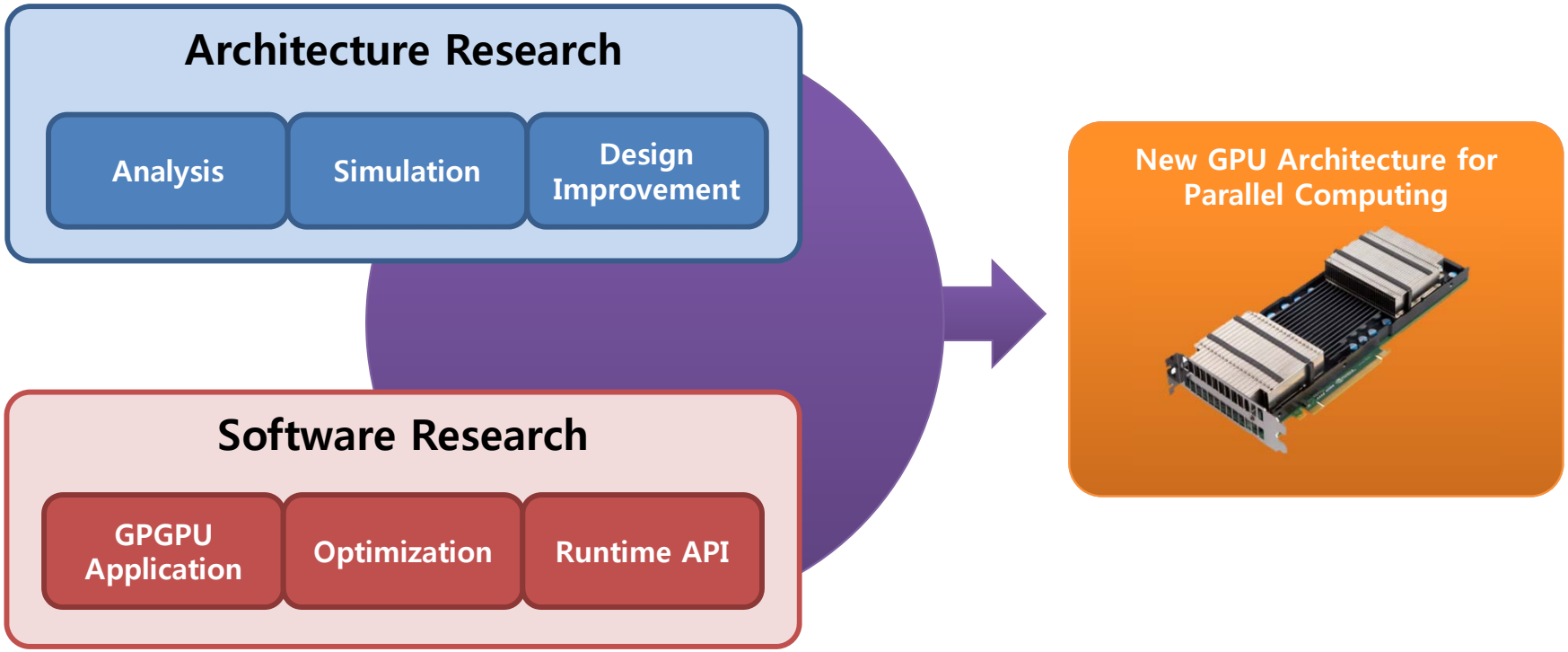
OUR CAPABILITY

- **GPU Architecture 및 Software 연구를 통한 GPU Architecture 개선**
  - ✓ Architecture 분석 및 simulation 기술
  - ✓ Simulation을 통한 GPU component 분석, architecture 개선을 통한 성능 향상
  - ✓ Software level 최적화를 통한 성능 향상, hardware utilization 향상



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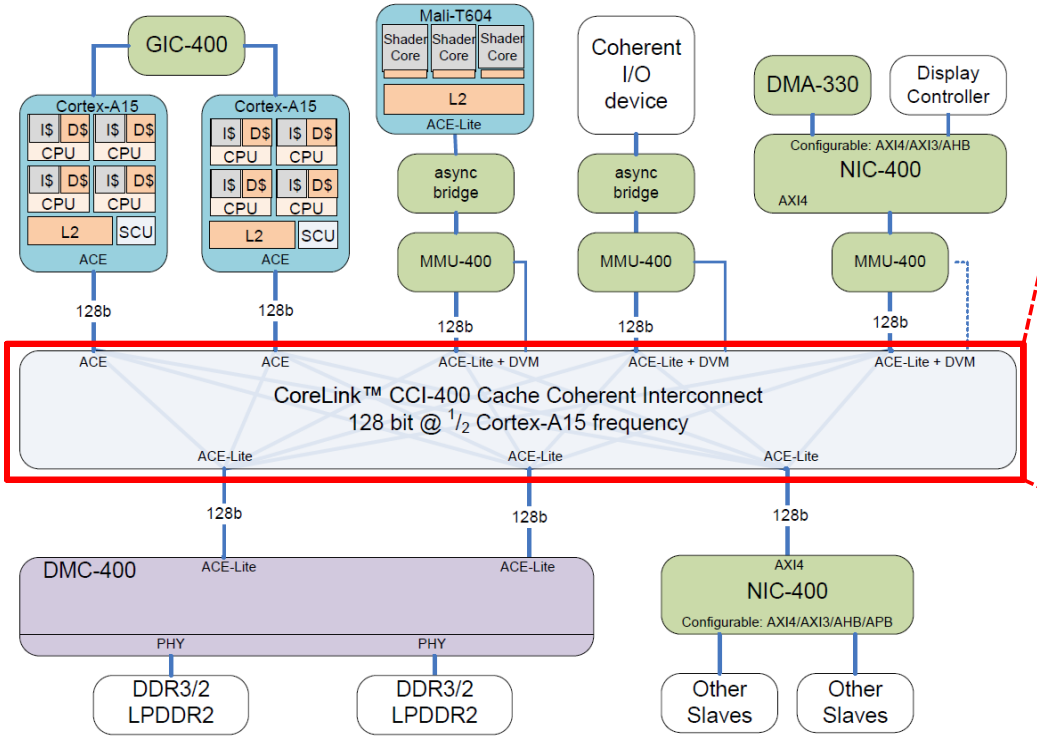
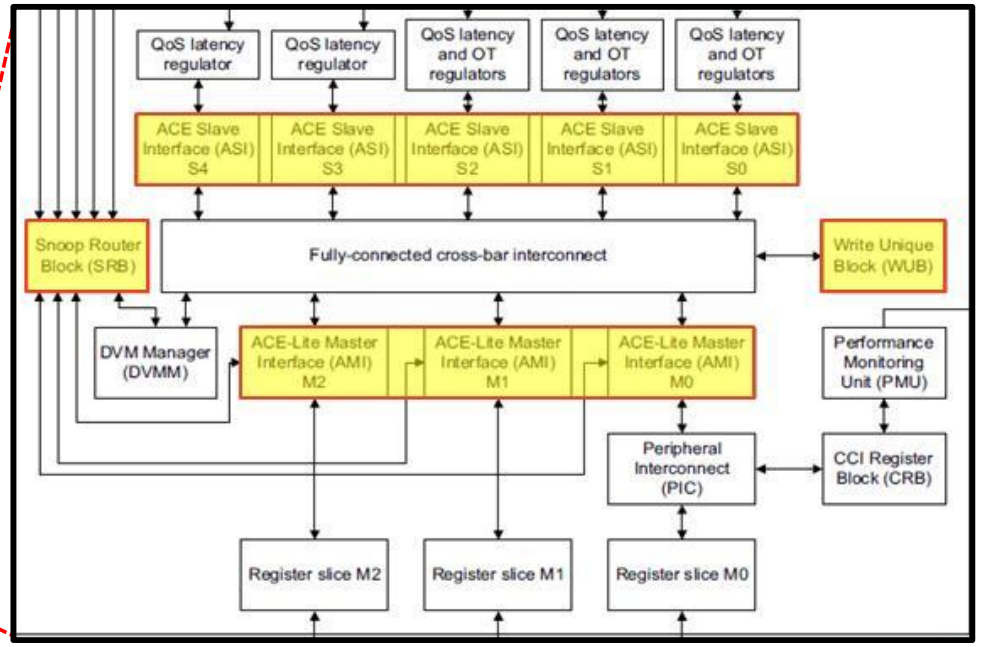
MOBILE AP INTERCONNECTION NETWORKS

- **Processor Core 및 Memory, 주변 장치 간 연결**
- **Multi-core Processor Cluster 간 Cache Coherency 지원**
  - ✓ Cortex™-A15 and Cortex™-A7
- **Example : ARM CoreLink CCI-400**





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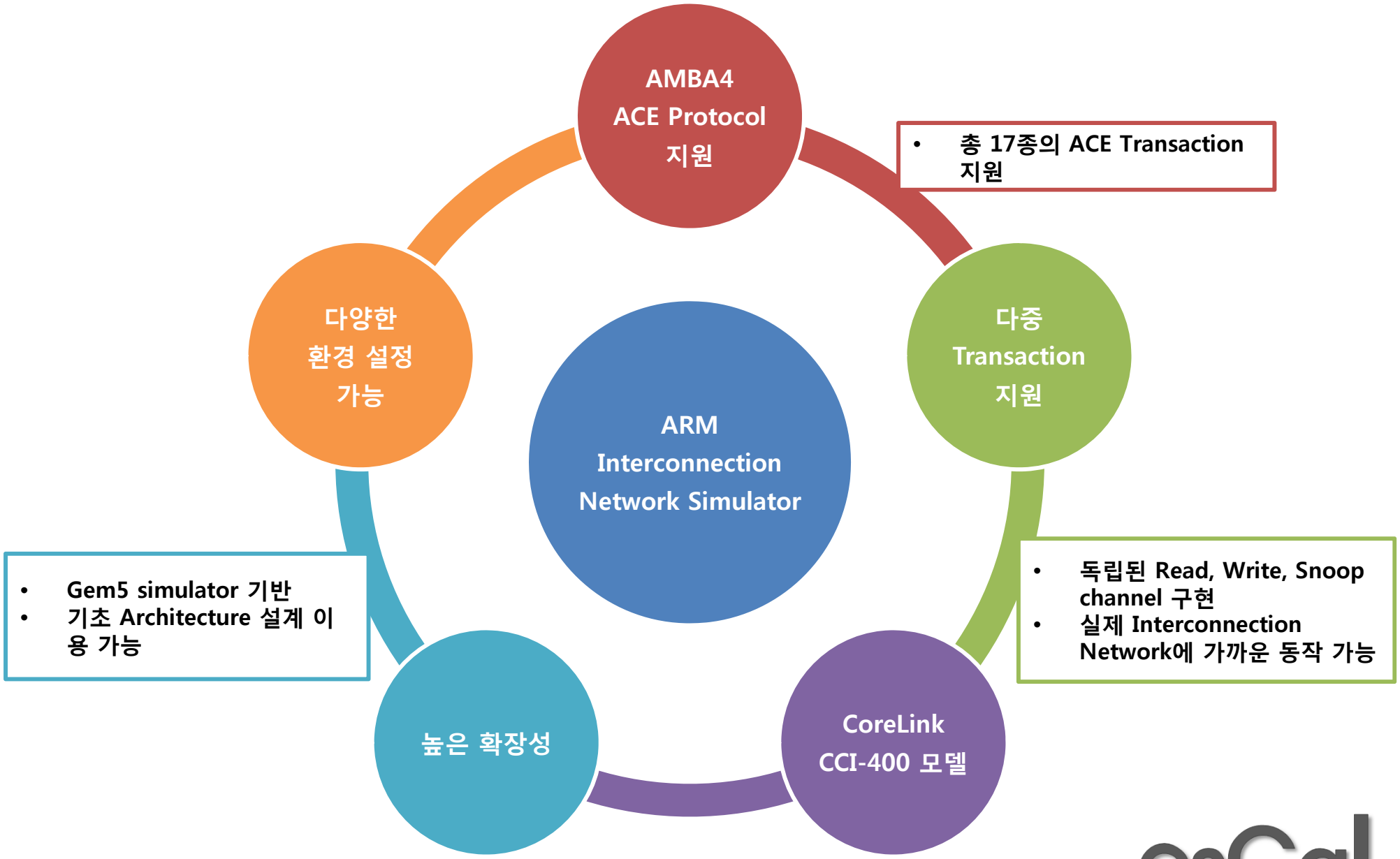
RESEARCH TOPIC – INTERCONNECTION NETWORK SIMULATOR



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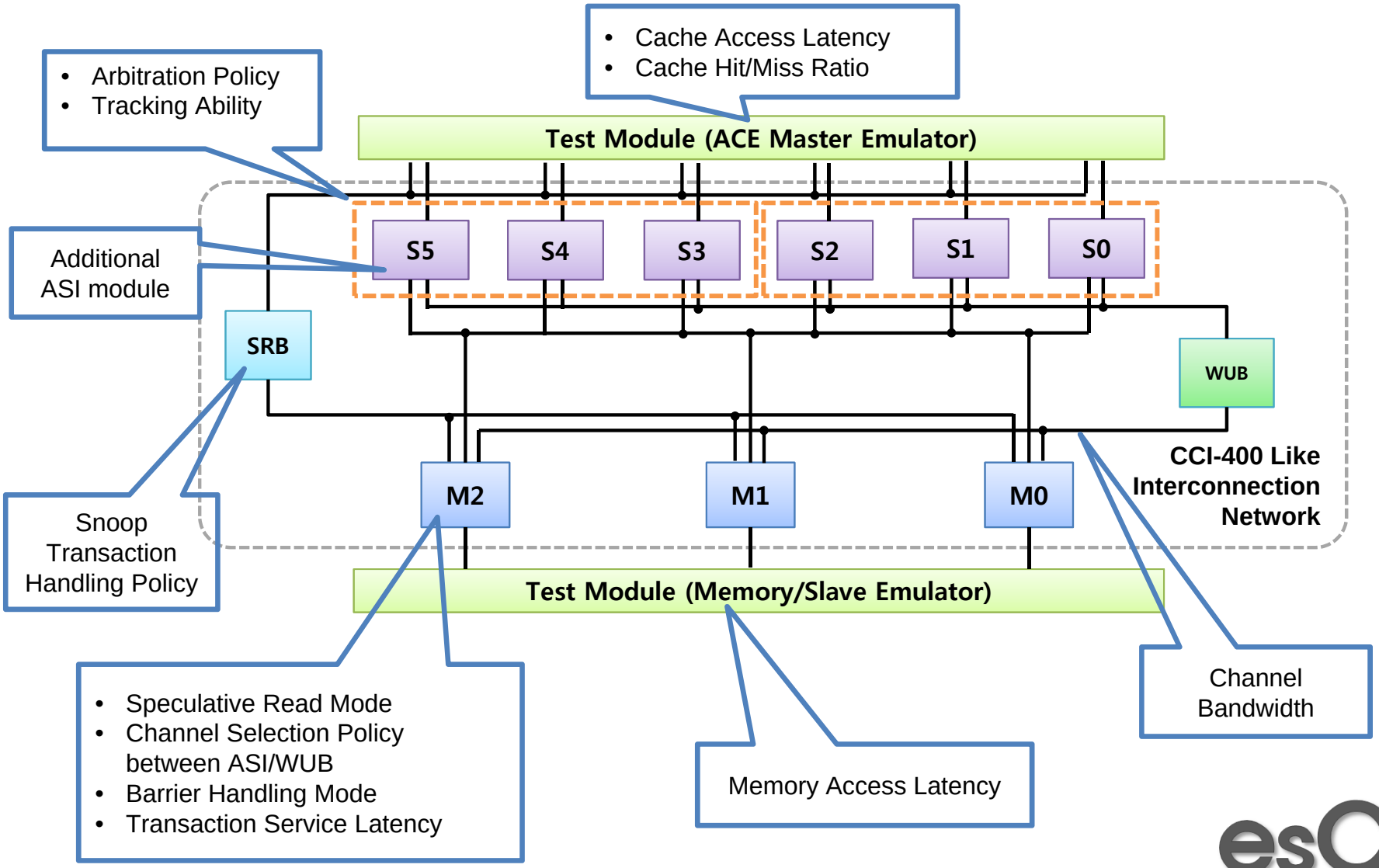
SIMULATOR CONFIGURABILITY

- **Interconnection Network 구성에 대한 다양한 설정 및 Simulation 가능**



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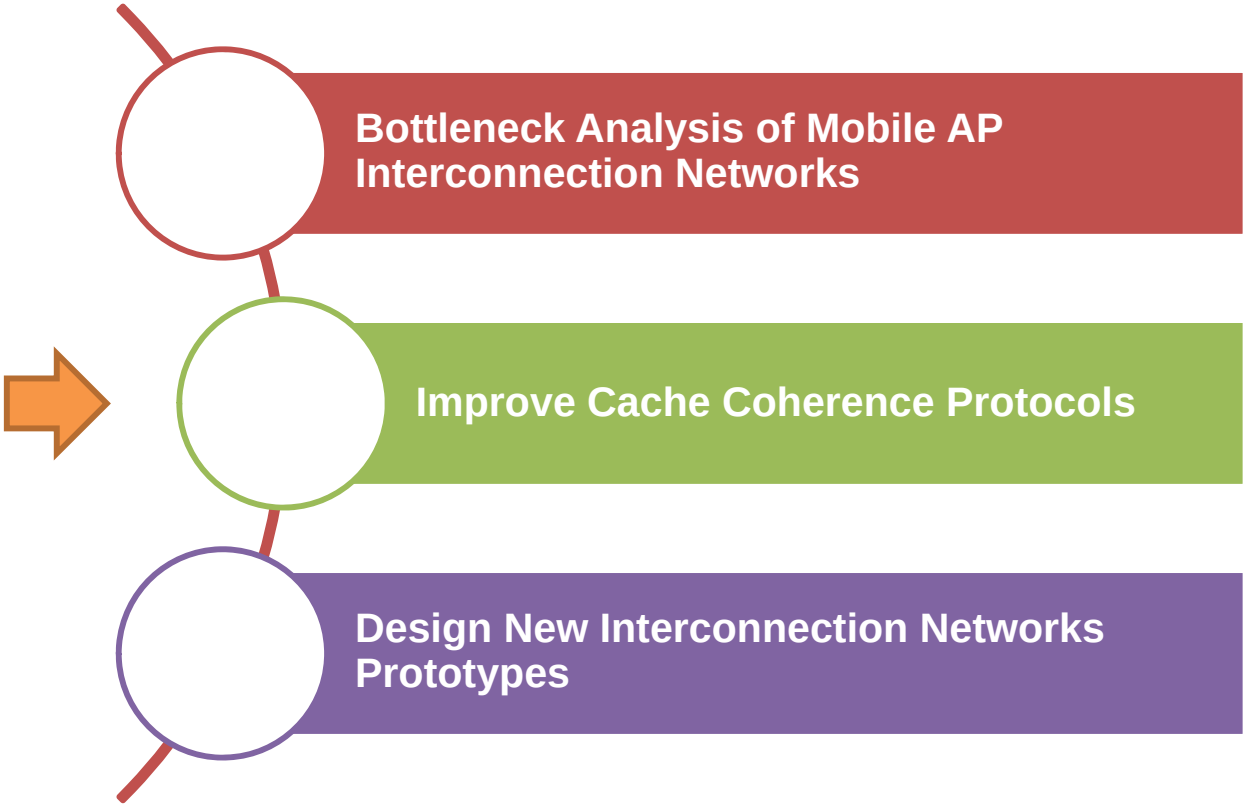
Our Capability

Experience about

- **ACE Protocol Implementation**
- **Interconnection Network Simulator**



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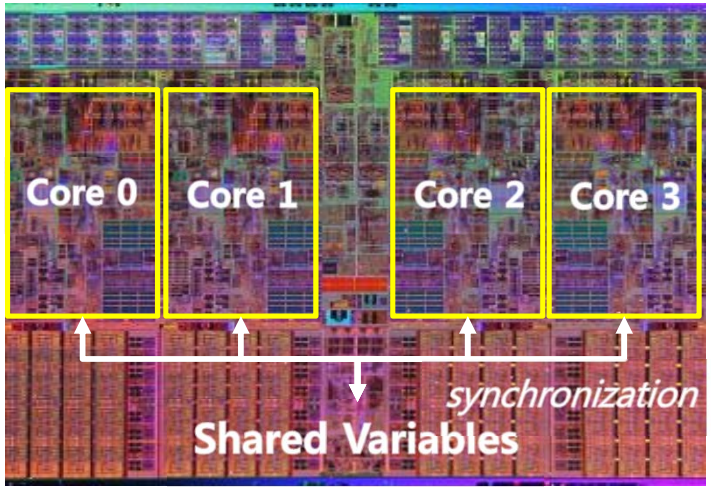
HARDWARE TRANSACTION MEMORY SYSTEMS

- **상호 배제(Mutual Exclusive) 특성이 없는 데이터 동기화를 위한 Architectural Support**

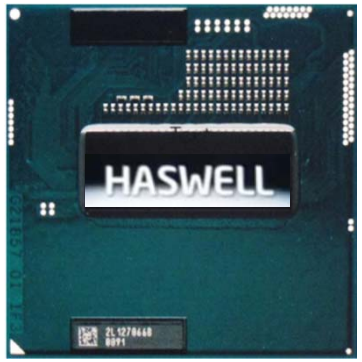
- **Lock 방식의 동기화 문제 해결**
  - ✓ Deadlock/Livelock 제거
  - ✓ 프로그램의 병렬 실행성능 향상

  → 멀티 코어 활용의 효율성 증가



- **트랜잭션의 정의**
  - ✓ A finite sequence of machine instructions executed by a single process.
  - ✓ 트랜잭션 실행의 Atomicity와 Serializability 보장을 통한 데이터 동기화

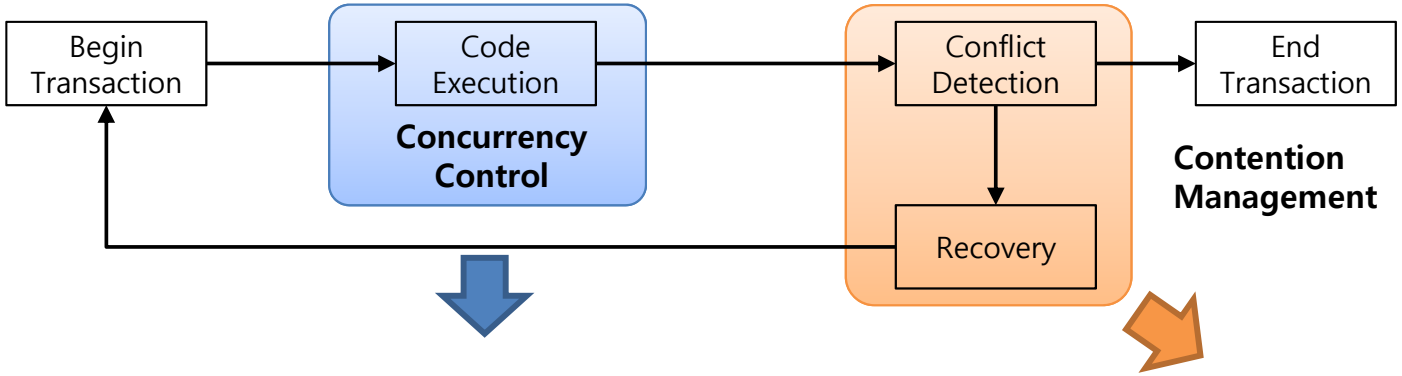
- **차세대 Intel Architecture(Haswell)에 적용**
  - ✓ Transactional Synchronization Extensions (TSX) 명령어 셋 추가를 통한 구현



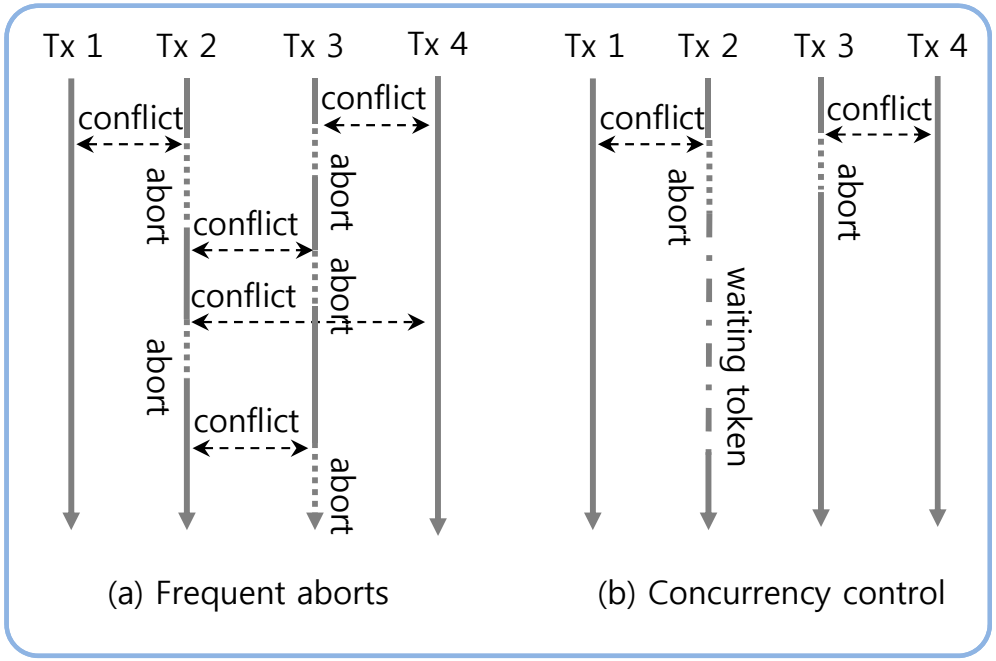
RESEARCH TOPIC

Contention Management and Concurrency Control

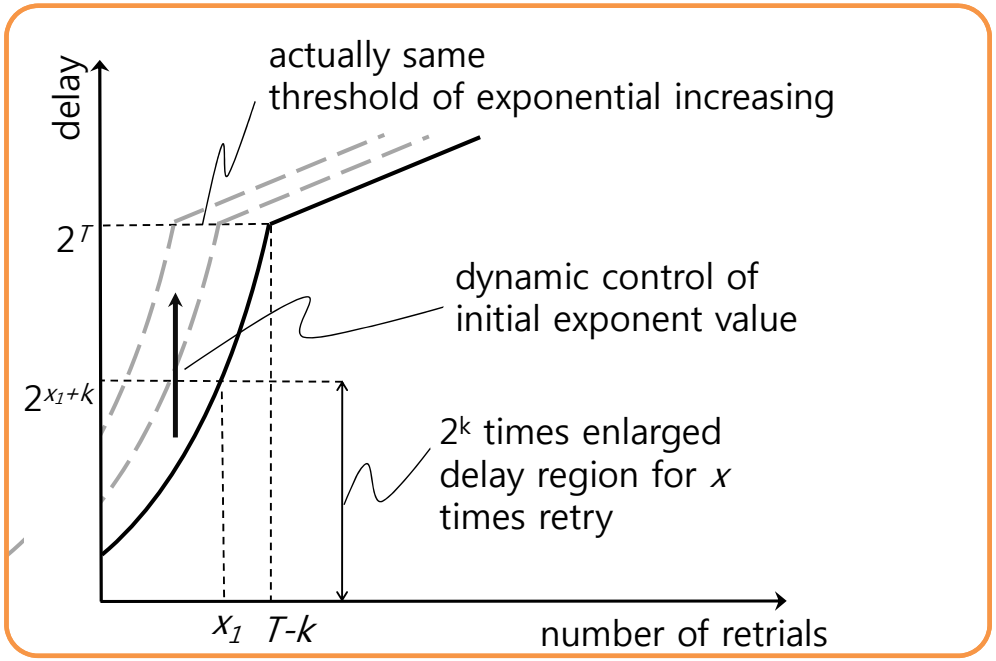
✓ 트랜잭션의 흐름



✓ 동시 실행 트랜잭션의 수 조절을 통한 성능 향상 연구



✓ Contention 양을 고려한 Back-off 알고리즘 연구



OUR CAPABILITY

- **모바일 기기의 멀티코어 적용 확대**

코어 수 증가에 따른 효율적
병렬 처리 구조 필요성 증가

- **Hardware TM Architecture 연구 방안**

✓ TM 연구 기술을 바탕으로 한 하드웨어 설계 및 검증